APPLICATION NOTE

TEA6880H, Car Radio Audio Signal Processor (front end part)

AN97023

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Abstract

The Car radio Audio Signal Processor TEA6880H (CASP) is a monolithic bipolar Integrated Circuit (IC) providing the stereo decoder function, weak signal detectors and controls, noise blanker (AM and FM) and tone / volume control for car radio use. It is I^2C bus controlled and needs no manual alignment.
The focus of this report is set to the stereo decoder, weak signal and noise blanker functions (front end).
In addition to this report, AN96085 gives a guide line for CASP soft ware design (tone / volume part).

Purchase of Philips I^2C components conveys a license under the Philips I^2C patent to use the components in the I^2C system, provided the system conforms to the I^2C specifications defined by Philips.

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Summary

This report is intended to provide application support for designing car radio receivers with the TEA6880H (mask version V1C) integrated circuit for stereo decoding, noise blanking (AM / FM) and weak signal processing. The tone / volume part of the IC is not subject of this report.
First a general circuit description is given, followed by a brief description of all settings which are under I^2C bus control. Finally there are shown some results carried out with help of a tuner module built up with the integrated AM / FM receiver TEA6840H (NICE). The used mask version of NICE is V1C.

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TEA6880H, Car Radio Audio Signal Processor (front end part)

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1. Introduction

The Car radio Audio Signal Processor TEA6880 (CASP) is a monolithic bipolar Integrated Circuit (IC) providing the stereo decoder function, weak signal detectors and controls, noise blanker (AM and FM) and tone / volume control for car radio use. It is I^2C bus controlled and needs no manual alignment.
The focus of this report is set to the stereo decoder, weak signal and noise blanker functions (front end). The feature content of the front end part is as follows:

- separated current driven signal inputs for AM and FM
- input for demodulated AM stereo signals
- voltage controlled PLL-oscillator (228 kHz) syncronized by an external reference frequency provided by the TEA6840H receiver IC
- pilot canceller
- input for RF/IF level signal (from level detector of the receiver, e. g. TEA6840)
- detectors for ultra sonic noise (USN) and wideband AM noise (WBAM)
- analog control of soft mute for off station noise
- analog control of stereo blend (SNC)
- analog control of high cut (HCC)
- FM noise blanker driven from RF/IF level and MPX signal
- AM noise blanker with separated inputs for (delayed) signal path and (undelayed) detector path
- A to D converter for level information (6 bit)
- A to D converter for USN and WBAM information (3 bit each)

2. General description

Besides the Tone / Volume part, which is not subject of this report, CASP contains FM stereo decoder with FM and AM mono signal path and additional signal inputs for an external AM stereo source, highly flexible detectors and controls for weak signal handling and ignition noise blanking for AM and FM. All alignments and settings, such as channel separation, detector sensitivity or control start and slope are I^2C bus controlled and no manual alignment is needed. A block diagram is shown in fig.1. The integrated circuit can be operated in ambient temperature range of -40 to 85^{o}C and supply voltage range 7.8 to 9.2V.

2.1 Stereo Decoder, Signal Path (see fig.2)

The MPX input (pin 57) is a "null-node" of an operational amplifier with internal feedback resistor. Adapting the signal source (FM demodulator) to the input of the stereo decoder can easily be done by choosing the series resistor between FM demodulator output and pin57. With R_s=182 kΩ the typical input voltage is 670mV_{RMS} for 100% modulation (deviation $\Delta f = \pm 75$kHz). A typical compensation for demodulator roll off can be done by a capacitive bypass to a part of the series resistor (see fig. 1). Separation alignment is provided by an internal boosting circuit for the S-signal with 9 steps (10 positions; data byte ALGN1, bit CHS0...CHS3) of 0.2dB each.
The input amplifier is followed by an integrated 8th order Bessel low pass filter with a cutoff frequency of 80kHz. It provides signal delay (6.5 μs) for FM noise blanking and damping of high frequency interferences coming to the stereo decoder input under multipath or neighbouring signal conditions at the antenna of the radio.
AM mono signal input (pin 52) again is the “null node” of an operational amplifier. With a series resistor the gain for the AM signal path can be set to the desired ratio of AM and FM AF output. The AM signal is fed from

the input amplifier via the AM noise blanker gate to the Bessel low pass filter into the FM channel and there both signals are combined.
From the output of the filter the signal is fed through the pilot cancelling circuitry (see chpt. 2.2) to the soft mute attenuator and the multiplex decoder. There, the side-signal is demodulated and combined with the main signal in a matrix to the left and right audio channel. In the 38kHz subcarrier signal, used for MPX-demodulation, the 3rd harmonic (114kHz) is cancelled out to prevent for demodulation of interfering signals around 114kHz. Interfering signals around the 5th harmonic are reduced by the Bessel filter at the input. Slope and starting point of the mute attenuator can be set by 2bits each (slope: data byte ALGN2; bit MSL1 and MSL0; start: data byte ALGN0, bit MST1 and MST0).
From the output of the MPX demodulator the signals are fed to the FM noise blanker gates (chpt.2.3) which are combined with the high cut poles (pins 61, 62). The de-emphasis is defined after the gates by internal resistors and the external capacitors at pins 59 and 60. With 3.3nF a nominal de-emphasis of 75µs is achieved. Switching to 50µs can be done by I^2C bus (data byte ALGN3, bit DE75).
From the de-emphasis the signal is fed to the output operational amplifiers. The outputs of these amplifiers are internally connected to the source selector. The output signal can be externally measured at the source selector output pins 13 and 27 (ROPO / LOPO) in case of switching the source selector to AM/FM. To handle overmodulation there is a built in headroom of +6 dB in the signal path.

2.2 Stereo Decoder, Subcarrier Regeneration

To regenerate the 38kHz subcarrier a PLL is used. The fully internal oscillator runs at 228 kHz and is alignment free with help of an external supplied frequency of 75.4 kHz (pin 48) as reference. The reference frequency is generated in the TEA6840 receiver IC. If no TEA6840 is used the reference frequency must be supplied from an external reference oscillator. The oscillator output signal is fed to the logic block, where the needed 19 kHz and 38 kHz signals are generated by division.
The 19kHz quadrature phase signal is fed to the 19 kHz phase detector where it is compared with the incoming pilot tone. In this signal the 3rd harmonic is cancelled to prevent for demodulation of signals around 57kHz, such like RDS (radio data system) or VF (Verkehrsfunk).
Normally, the DC output signal of the phase detector, used to control the oscillator (PLL), is superposed by an offset caused by spreads of the internal circuitry. This offset influences the free running frequency of the oscillator and thus the catching and holding range of the PLL. In conventional stereo decoders this offset is aligned together with the alignment of the R/C oscillator. Using an oscillator with no alignment the offset has to be compensated. In CASP, with help of internally circuitry, the offset is converted into an AC signal (19kHz) and rejected by the external loop filter (pin 47). Due to the compensation an only one-pin loop filter can be used.
The pilot presence detector is driven in parallel to the phase detector but with internally generated in-phase 19 kHz. The pilot level dependent DC output voltage (pin 49) of the pilot presence detector is fed to a threshold switch, which activates the pilot indicator logical output (I^2C bus) and turns the stereo decoder into stereo operation. The same DC voltage (pin 49) is used to control the amplitude of an anti-phase internally generated 19kHz voltage to the level of the pilot tone. In the pilot cancel circuitry the pilot tone is compensated by the anti-phase 19 kHz signal.

2.3 Noise Blanker (see fig.3)

2.3.1 FM Part

The noise blanker is internally connected to the MPX signal and in parallel to level from level buffer and filtered level from mute average detector. The MPX signal is fed via a 2-pole high pass filter to a full wave negative peak detector. Level and the filtered level are fed to a comparator and by an offset between both level signals, the noise floor of the level is cut. From the comparator the signal is fed via a 1-pole high pass to another full wave negative peak detector and then combined with the negative peak detected MPX signal. This combined signal is fed to the noise peak detector with a time constant defining external capacitor at pin58. With increasing noise (noise, modulation or other continuously present signals), the noise detector

generates an increasing offset at the interference detector and activates gain control for the input high pass amplifier of the MPX signal. This decreases the trigger sensitivity to prevent from false triggering at noisy (weak) input signals. The basic trigger sensitivity can be changed by 2 bits from the I^2C bus (data byte ALGN3: NBS1 and NBS0). Receiving steep pulses, the output of the interference detector fires a monoflop, contained in the pulseformer circuitry. The time constant of the retriggerable monoflop (blanking time) is defined internally. The output of the monoflop activates the FM blanking gates in the AF signal path.
To prevent from false triggering, caused by higher modulation, there is in addition a modulation detector built in, which controls the gain of the MPX detecting path.
In case of high pulse repetition frequency (> 2 kHz) the noise blanker is defeated by an extra control loop.

2.3.2 AM Part

The AM noise blanker detector is driven from the undelayed AM AF signal (input at pin 53). This input must be DC coupled to the AM demodulator output of the receiver, DC voltage should be in the range of 3 to 6 V. The AM AF signal path has to be delayed by an external delay line with about 150 µs and than fed via a series resistor into pin 52. The pulse detector is a peak-to-average detector (pin 25) with a threshold corresponding to positive modulation of 140%. A pulse coming through this detector fires a one shot monoflop with an external time defining capacitor (pin48). The output signal of the pulse former controls the AM gate in the AM signal path.
For AM stereo the external gates (part of the AM stereo decoder) can be controlled from pin 42 (noise blanker flag). Different gating times can be met by choosing the capacitor value at pin 41.

2.4 Weak Signal Control (see fig.4)

To control soft mute, stereo blend (SNC) and high cut (HCC), there are built in four negative going detectors:

- Mute / HCC average detector is driven from level buffer output. The attack and decay time of the detector is 1 s with an external capacitor of 220 nF at pin 54. Output voltage versus level input voltage is shown in fig.5.
- ultra sonic noise (USN) average detector is driven from the MPX signal via a 2-pole 80 kHz high pass filter. The attack and decay time is 1 ms with an external capacitor of 4.7 nF at pin 64. The output voltage of the detector is limited to 2 V. This limits the effect on the controls to this value. Sensitivity (gain) of the detector can be set by 2bits (data byte ALGN1: USS1, USS0). Characteristic is shown in fig.6.
- wide band AM (WBAM) average detector is driven from the level buffer output via a 20 kHz band pass filter. The attack and decay time is 1 ms with an external capacitor of 4.7 nF at pin 63. The output voltage of the detector is limited to 2 V. This limits the effect on the controls to this value. Sensitivity (gain) of the detector can be set by 2bits (data byte ALGN1: AWS1, AWS0). Characteristic is shown in fig.7.
- SNC peak detector is driven from the level buffer output, the USN high pass output and the WBAM band pass output in an “OR” combination (see). The attack time is 400 ms and the decay time is 10 s with an external capacitor of 10 µF at pin 56. Chararcteristics are shown in fig.5, 6, 7.

Mute / HCC average detector and SNC peak detector can be set to faster by a test bit (data byte TRBL, bit HSTM). When tuning the radio, the slow detectors can be set faster by data byte ALGN0, bit SEAR. The following table gives an overview over the combinations of the sources to the controls.

.

dependency **of** / **on**	**MUTE**	**SNC**	**HCC**
LEVEL	slow average detector	slow peak detector	slow average detector
USN	quick average detector	slow peak detector & quick average detector	—
WBAM	—	slow peak detector & quick average detector	—

Table 1: Weak signal processing, dependencies on sources

2.4.1 Soft Mute Control

Soft mute control is driven from the Mute / HCC average detector and the USN detector in an “OR” combination. By this occasionally steep pulses are practically blanked by the USN detector signal and more static fading is followed by the slow average detector driven from level. Off station noise and start of muting are defined by the RF/IF input level dependent signal at the level buffer output. The level voltage, provided by the receiver TEA6840 (NICE), is aligned in absolute value and slope. Starting point and slope of the soft mute control can be set by I^2C bus with 2 bits each (starting point: data byte ALGN0, bit MST1 and MST0; slope: data byte ALGN2, bit MSL1 and MSL0) . The mute control curves are given in fig. 8 and 9.
The soft mute also can be used in AM mode with the same or different bus settings. If this is not wanted the soft mute control can be swtiched off by bit SMUT in data byte ALGN0.
The soft mute control provides additional a deep mute (80 dB) controlled by I^2C bus (data byte ALGN0, bit MMUT). For this function the time constant of the USN average detector is valid.

2.4.2 Stereo Noise Control (stereo blend)

Stereo noise control (SNC) is driven from the SNC peak detector, the USN average detector and the WBAM average detector in an “OR” combination. By this short noise or multipath pulses on stereo are practically blanked out, while at more severe and longer lasting noise and multipath or fading the SNC peak detector with its long time constant takes over the control to avoid stereo pumping.
Starting point and slope of the stereo / mono transition can be set (or if wanted aligned) by I^2C bus (starting point: data byte ALGN2, bit SST3...SST0; slope: data byte ALGN2, bit SSL1 and SSL0, (three positions only). Transition curves are given in fig. 10 and 11.

2.4.3 High Cut Control

High cut control (HCC) is driven from the Mute / HCC detector only.
Starting point and slope of HCC can be set by I^2C bs with 2 bits each (starting point: data byte ALGN3, bit HST1 and HST0; slope: data byte ALGN3, bit HSL1 and HSL0).
The maximum attenuation caused by high cut control is 10 dB at 10 kHz with 2.7 nF capacitors at pins 61 and 62. These capacitors, without HCC active, are forming a fixed pole with 5 dB static roll off at 10 kHz. If this roll off is not wanted, the capacitors can be set to 680 pF, then the static roll off is less than 1 dB, but HCC is practically defeated. Therefor with one bit (data byte ALGN3, bit HCCS) the internal high cut control circuit can be set to higher currents, so that maximum attenuation at 10 kHz is 10 dB again. HCC characteristics are given in fig. 12 and 13.

2.5 RDS Update

In the Radio Data System a list of alternative frequencies for a programm chain is transmitted. If the recieved station is fading out or is heavily distorted by multipath, the radio can be automatically tuned to an other station with the same programm but better level or less multipath. To get information about signal quality of the alternative frequencies the radio has to be tuned periodically to alternative frequencies to prove their signal quality. These test tunings have to be as less audible as possible. Tests carried out show that the gap in the signal should be no longer than 5 to 7 ms when soft muting flanks are used. Subtracting muting and tuning times a remaining time for signal quality testing is about 2 ms. Signal quality can be measured with help of three criteria:

- RF / IF level, A to D converted with 6 bit resolution
- Ultra sonic noise, peak detected (1 ms attack, 10 ms decay) and A to D converted with 3 bit resolution
- AM wideband distortion, peak detected (1 ms attack, 10 ms decay) and A to D converted with 3 bit resolution

To control the functions needed for RDS update in CASP there are pin51 (FMHOLD) and pin 50 (AFSAMPLE) available. For normal receiving FMHOLD is HIGH and AFSAMPLE is LOW. In table 2 the functional flow of a RDS update cyclus is given.

STATUS	FMHOLD pin 51	AFSAMPLE pin 50	RDSU (2nd. data byte READ)	Functional flow
normal receiving, continous mode	HIGH	LOW	LOW	USN and WBAM peak detectors are continously measuring and can be read out on request.
start of RDS update	LOW	LOW	LOW	weak signal detectors on hold USN peak detector on reset WBAM peak detector on reset
after muting and tuning to alternative frequency	LOW	HIGH	LOW	weak signal detectors on hold USN peak detector active WBAM peak detector active
after measuring time	LOW	LOW	HIGH	weak signal detectors on hold Level result stored USN peak detector result stored WBAM peak detector result stored
after storage time and tuning back to received station	HIGH	LOW	HIGH	weak signal detectors active Level result, USN and WBAM peak detector result stored until they are read out.
after reading out measuring results	HIGH	LOW	LOW	weak signal detectors active USN peak detector active WBAM peak detector active normal receiving, continous mode

Table 2: RDS update functional flow

2.6 A to D Converters

2.6.1 Level converter

The level A to D converter converts to 6 bit (63 steps). Conversion starts at 950 mV level input voltage with 000000 and has 63 equal steps of 47 mV ending at 3.86 V with 111111.
Assuming that the level from TEA6840H is aligned to 500 mV minimum (off station) and starts with contant (aligned) slope of 800 mV/decade at 1µV antenna voltage, the A toD converter covers a range of antenna input voltage from 3 µV to 15.9 mV (4.2 decades) with about 1.2 dB/step.
When the CASP is switched to AM or AM stereo mode by data byte ALGN0, bit AMON or AMST, the input of the A to D converter is switched to the output of the Mute/HCC average detector, which is only dependent on level, to remove the AM modulation from the A to D converter input.

2.6.2 USN and WBAM Converters

The USN and WBAM converters convert to 3 bit (7 steps) each. The 7 steps are equal with 340 mV each. 000 correspondends to 2.1 V, while 111 is related to 4.5 V. The relations to modulation degree for the single steps can be taken from the figures 6 and 7. The relation between a single step and the degree of modulation is dependent on the setting of the detector sensitivity (data byte ALGN1, bits USS1, USS0, AWS1, AWS0). These bits are also valid for the USN and AMWB average detector in the weak signal processing part.

2.7 I^2C Bus Controls

For the front end of CASP the bus protocol contains 2 data bytes for read mode and 4 data bytes for write mode.

2.7.1 Read Mode

The read mode data bytes are given in table3. They contain the output values of the signal quality A to D converters for level, ultrasonic noise and wideband AM noise. Additional in the 1st data byte bit STIN gives information about the status of the stereo indicator (HIGH = stereo on) and bit RDSU tells, when it is HIGH, that data of the A to D converters are from an RDS update, while, when RDSU = LOW, data are from continous mode measuring.

1st data byte							
STEREO INDICATOR	MEASURE MODE	LEVEL					
STIN	RDSU	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0
2nd data byte							
	ULTRA SONIC NOISE				WIDEBAND AM NOISE		
0	USN2	USN1	USN0	0	WBA2	WBA1	WBA0

Table 3: Data Bytes for Read Mode

2.7.2 Write Mode

The data bytes for write mode used for the front end part of CASP are shown in table 4.
With these bytes mainly the starting points, slopes and sensitivties of the weak signal handling can be set or aligned. The effect to these functions can be seen from figures explained in chpt. 2.4, but there are some bits which need to be described:

- data byte ALGN0, bit MONO: HIGH switches the stereo decoder to mono mode (forced mono).
- data byte ALGN0, bit MMUT: HIGH mutes the stereo decoder (80 dB) in FM and AM mode. The muting is done with the time constant of the USN average detector (same time for attack and decay). This muting can be used as preset tuning mute or RDS update mute when CASP is used without TEA6840H (NICE) as receiver.
- data byte ALGN0, bit SMUT: with this bit the soft mute can be switched of, e.g. in case of AM receiving.
- data byte ALGN0, bit SAER: with this bit, in case of seek or search tuning, the detectors with long time contsants (mute, SNC) can be set to quick response.
- data byte ALGN0, bit AMST: this bit sets CASP to AM stereo receiving. It must be used in combination with bit AMON set to HIGH.
  Then is:
  VCO of the PLL switched off
  stereo decoder set to mono
  pilot canceller switched off
  de-emphasis disabled and pin61, 62 set to input mode
  stereo decoder set to mute (80 dB)
  input of level ADC switched to Mute/HCC average detector output
- data byte ALGN0, bit AMON: this bit stes CASP to AM mono receiving. That means:
  VCO of the PLL switched off
  stereo decoder set to mono
  pilot canceller switched off
  input of level ADC switched to Mute/HCC average detector output
  input of 80 kHz low pass filter switched to output of the AM gate
- data byte ALGN3, bit HCS: this bit adapts the range of HCC when applying 680 pF instead of 2.7 nF to pins 59, 60

.

data byte ALGN0							
AM/FM SWITCH	AM STER SWITCH	SEARCH MODE	SOFT MUTE	MPX MUTE	MO/ST MODE	SOFT MUTE STARTING POINT	
AMON	AMST	SEAR	SMUT	MMUT	MONO	MST1	MST0
data byte ALGN1							
ULTRA SONIC NOISE SENSITIVITY		WIDE BAND AM SENSITIVITY		CHANNEL SEPARATION ALIGNMENT			
USS1	USS0	AWS1	AWS0	CHS3	CHS2	CHS1	CHS0
data byte ALGN2							
MUTE SLOPE ADJUSTMENT		SNC (BLEND) SLOPE ADJUSTMENT		STEREO NOISE CONTROL (BLEND) START ADJUSTMENT			
MSL1	MSL0	SSL1	SSL0	SST3	SST2	SST1	SST0
data byte ALGN3							
NOISE BLANKER SENSITIVITY		DEEM-PHASIS	HIGH CUT CTRL SW.	HIGH CUT CONTROL START ADJUSTMENT		HIGH CUT CONTROL SLOPE ADJUSTMENT	
NBS1	NBS0	DE75	HCCS	HST1	HST0	HSL1	HSL0

Table 4: Data Bytes for Write Mode of the CASP Front End

3. Settings and alignments

To set or align the different bits in the CASP front end a flow is proposed to get started.

3.1 Level curve.

Assumption for all settings and alignments of the weak signal processing part is a defined level curve versus antenna input voltage provided by the receiver. The tresholds and slopes designed into TEA6880H are based upon an off station level of 500 mV, a slope of 800 mV/decade of input signal and start of level information at 0.8 μV EMF or 5 dBf at 50 Ω impedance (see fig.14)

3.2 Soft mute

3.2.1 Setting

First step for settings should be the soft mute. With the level signal connected to pin3 the setting for desired α_{-3dB} and for off station noise should be made with help of data byte ALGN0 bits MST1, MST0 (fig. 8) and data byte ALGN2 MSL1, MSL0 (fig. 9). These bits are meant as system parameter settings and not for alignment.

3.2.2 Alignment

Looking at the complete system with TEA6840H as receiver and TEA6880H as backend (NICE and CASP) in the low level region (V_{ANT} = 1...5µV) there are four specification items of the radio to be aligned and influenced by the level.

1.α_{-3dB}

2.off station noise

3.start of keyed AGC

4.stop level

Item 1...3 are in a fixed relation and, after setting of the soft mute bits, can be aligned by the level start in NICE. Alignment can be done to a fixed DC level voltage at a fixed RF input signal or to one of the three items, the choice of which depends on what the most important specification is.
Stop level can be set after level alignment by software out of the 63 steps of the level A to D converter.

3.3 Channel separation

3.3.1 Setting

After level (soft mute) alignment a typical radio should be set to maximum channel separation at V_{ANT} > 1 mV by choice of the value of the parallel capacitor to a part of the input series resistor in front of pin57 (MPX input). For this setting the channel separation alignment bits (data byte ALGN1, bits CHS3...CHS0) should be set to a mid position.

3.3.2 Alignment

After the setting production spreads can be aligned by bits CHS3...CHS0 of data byte ALGN1 to maximum channel separation.

3.4 **Stereo noise control** (stereo blend)

3.4.1 Setting

With help of the bits SSL1, SSL0 for slope (fig. 10) and SST3 to SST0 for start (fig. 11) in data byte ALGN2 the radio can be set to the desired slope and start of the level dependent mono / stereo transition. Start of stereo blend (α_{sep}=10dB) with the proposed level curve can be set in a range from about 30µV at the generator (37dBf at the product) to about 180µV (52dBf) antenna voltage.

3.4.2 Alignment

Normally start of stereo blend is aligned by the aligment of level slope in NICE, but optional also in CASP start of stereo blend can be aligned for production spreads.

3.5 High cut control

Start of high cut is set by bits HST1 and HST0 in data byte ALGN3 (fig. 13), while the slope of the transition is set by bits HSL1 and HSL0 in data byte ALGL3 (fig. 12). This are system settings and automatically aligned together with soft mute and stereo blend.
In the typical application with 2.7 nF at pins 61, 62 the circuit has -5 dB static roll off at 10 kHz and additional -10 dB attenuation by high cut control. When the static roll off is not wanted, the capacitors at pins 61, 62 must be changed to 680 pF, the static rolloff then is < 1dB, but high cut attenuation range is decreased. To set this range back to -10 dB, the bit HCS in data byte ALGN3 must be turned from HIGH to LOW.
Capacitors at pins 61, 62 should not be less than 680 pF because they are additionally used as sample and hold capacitors for the FM noise blanker.

3.6 Ultra sonic noise and AM wide band sensitivity

Sensitivity of USN and AMWB channel can be set by bits USS1, USS0 (fig. 6) and AWS1, AWS0 (fig. 7) in data byte ALGN1. These are system settings and do not need to be aligned. Settings are influening the dynamic controls of soft mute and stereo blend. Optimized settings for a radio development should be carried out with help of multipath simulations or fieldtests.

3.7 FM noise blanker

With help of bits NBS1 and NBS0 (data byte ALGN3) the basic trigger sensitivity can be set. These are system settings and do not need to be aligned. Optimized setting is strongly dependent on system parameters, such as IF selectivity (IF filter types) and must be carried out with help of ignition pulse simulations and fieldtests. With NBS1=1, NBS0=1 the circuit is less sensitive, with NBS1=0, NBS0=0 the circuit is more sensitive.

3.8 De-emphasis

By bit DE75 in data byte ALGN3 de-emphasis can be switched from 75 µs (DE75 = 1) to 50 µs (DE75 = 0).

4. Application

4.1 General

Figure 15 shows the complete application circuit with a tuner module built up with TEA6840H (NICE). It includes the additional external circuitry needed for AM noise blanker. IF no AM noise blanking is wanted, the elements of the delay line (2 transistors, 5 capacitorsand 6 resistors plus the capacitors at pins 25, 41, 43 can be saved. In that case pin 53 (AMNBIN) should be connected direct to pin 44 (IREF) to prevent the blanker from firing.
The parallel capacitor (33pF) to 100kΩ resistor at the MPX input defines compensation of roll off caused by the FM IF selectivity (ceramic filters) and demodulation. In this case the value is optimized for use of two ceramic filters with 180 kHz bandwidth and one filter with 240 kHz bandwidth. For different filters the capacitor value needs to be changed. More narrow filters need higher capacitance value.
The resistor value (160 kΩ) at pin 52 (AM mono input) defines the relation between AM and FM audio output levels. It is set such, that 90% AM modulation matches to 67.5 kHz deviation at FM.
The values of the time defining capacitors at the detectors for weak signal processing (pins 54, 56 63, 64) are proposed, and can be changed in a wide range if different timing is wanted. Attack and decay times are direct proportional to the capacitor values.
Bus inputs (pins 4 and 5) need to be pulled up by external resistors. these are not contained in the diagram because they are normally at the µ–processor.
CASP has 2 bus adresses. They can be choosen by pin15 (adress select). In the diagram pin15 is connected to ground (adress Hex 18). If pin15 is left open adress Hex 19 is selected.

4.2 Results

- Figure 16 shows the static weak signal bahaviour with a proposed setting of mute, SNC and HCC thresholds and slopes. All settings are based upon the aligned level curve from the tuner module. Ultimate signal to noise ratio of only 53 dB is caused by inperfection of the current version of the receiver IC TEA6840H.
- Figure 17 shows FM AF response with pre-emphasis and channel separation versus modulation frequency. It shows the 5 dB static roll of at f = 10 kHz with 2.7 nF at pins 61 and62.
- Figure 18 shows FM noise blanker performance versus antenna voltage. Pulses are applied with

  140 mV amplitude
  1 µs duration
  < 6 ns rise and fall time
  3 ms repetition time

- Figure 19 shows the SINAD measurement versus antenna voltage with and without ignition pulses at the antenna input.
- Figure 20 shows the AM AF response versus modulation frequency.

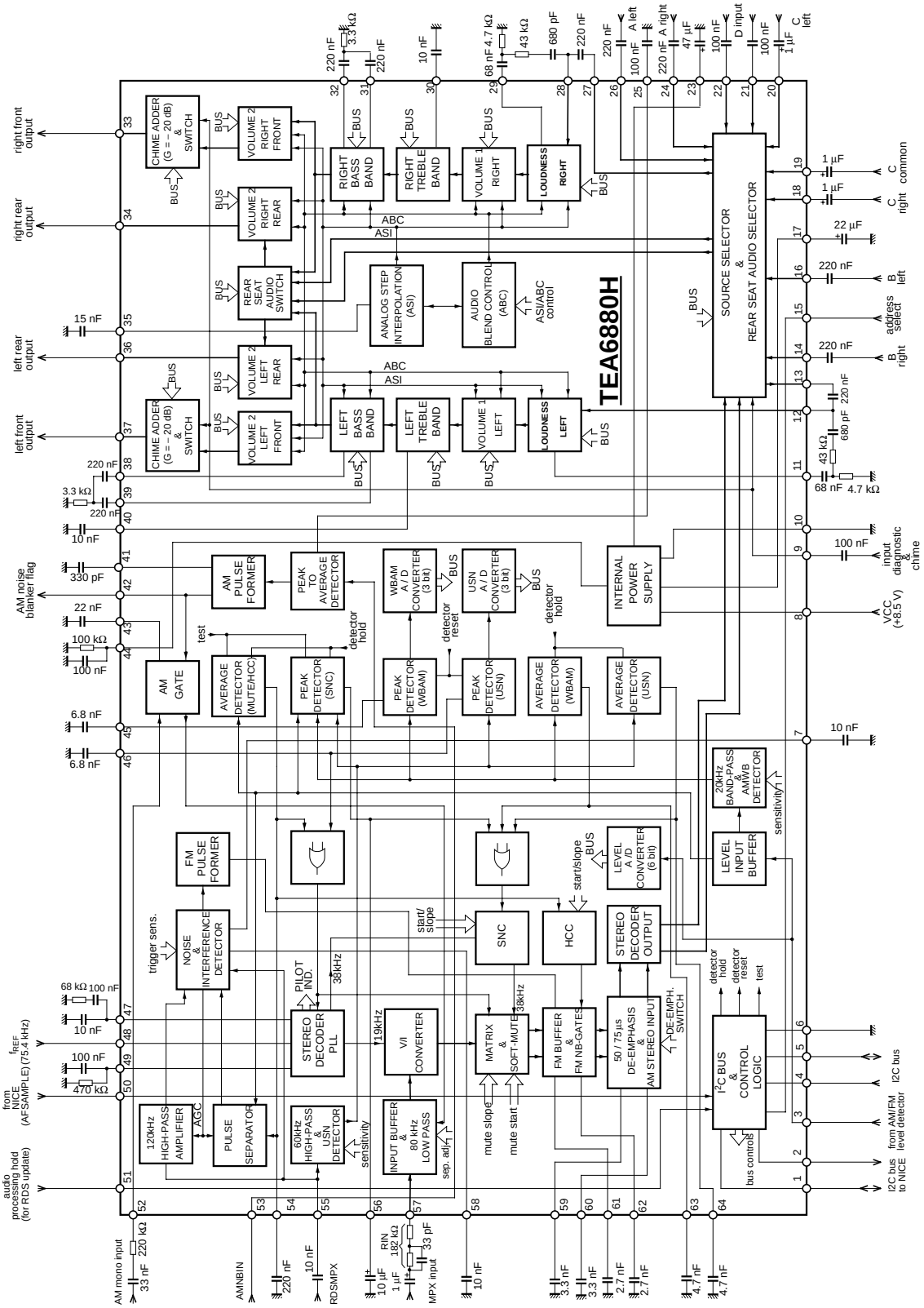


Fig.1 Block diagram of TEA6880H (CASP)

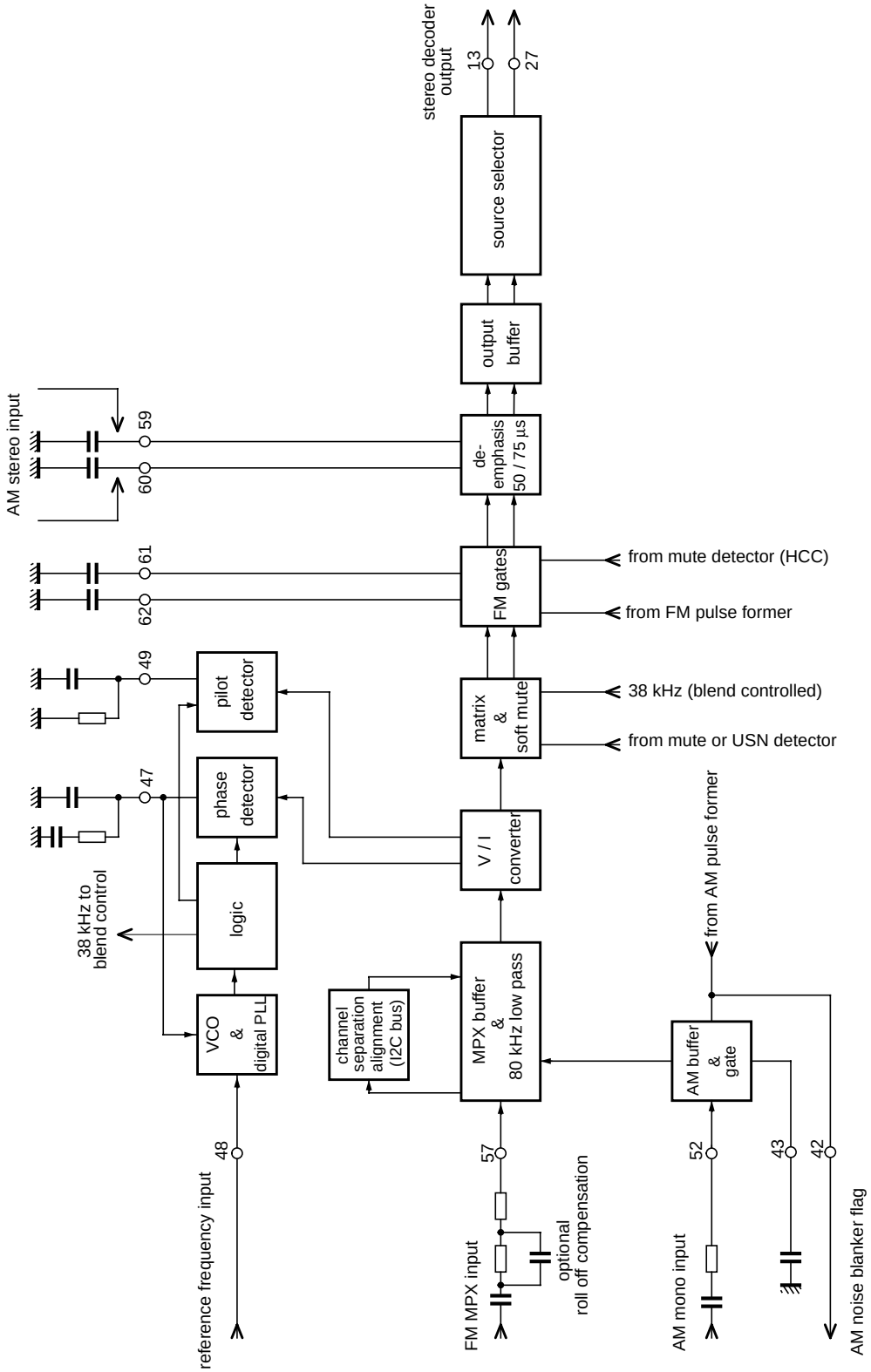


Fig.2 Block diagram of signal path

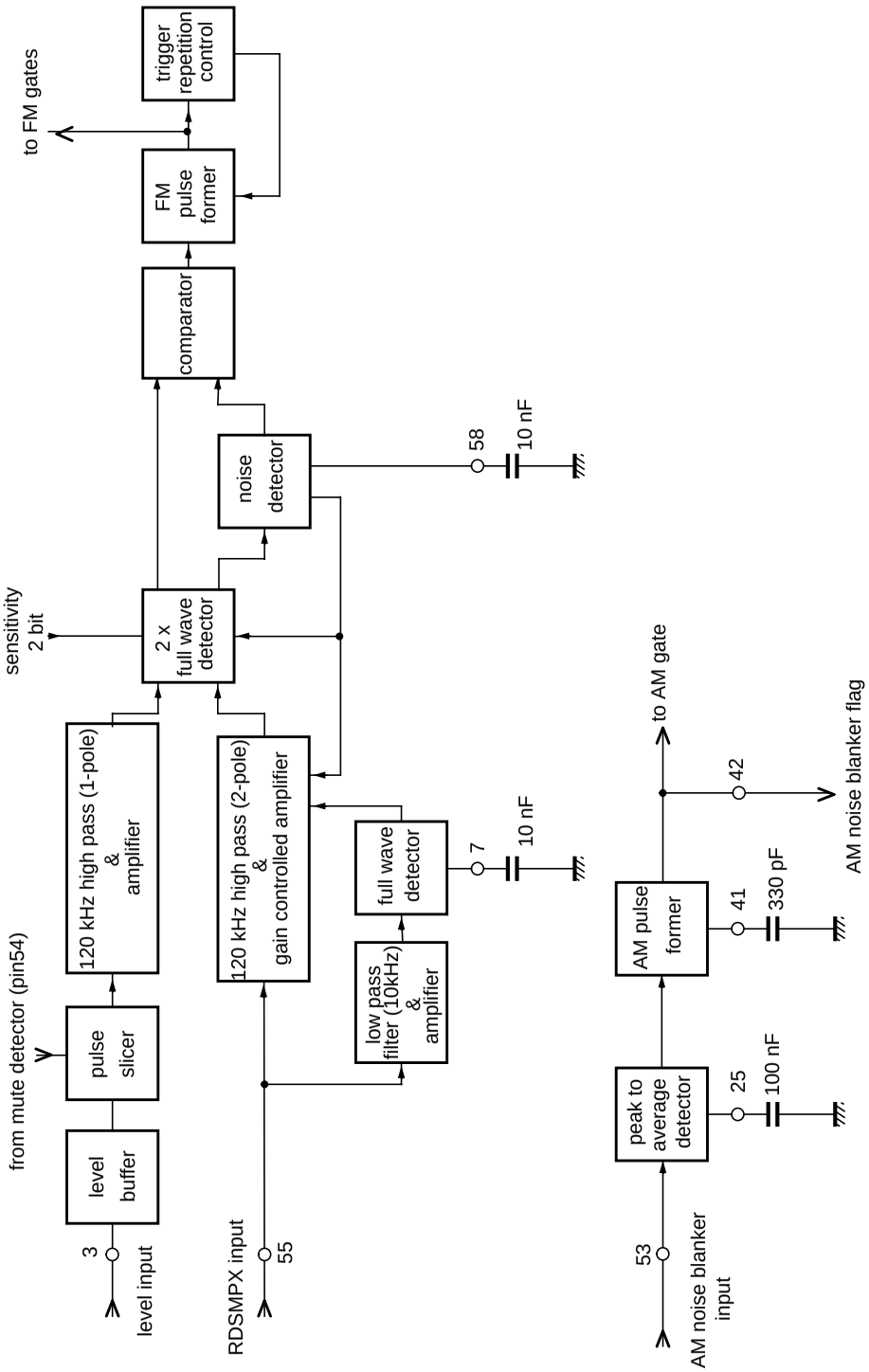


Fig.3 Block diagram of the noise blanker

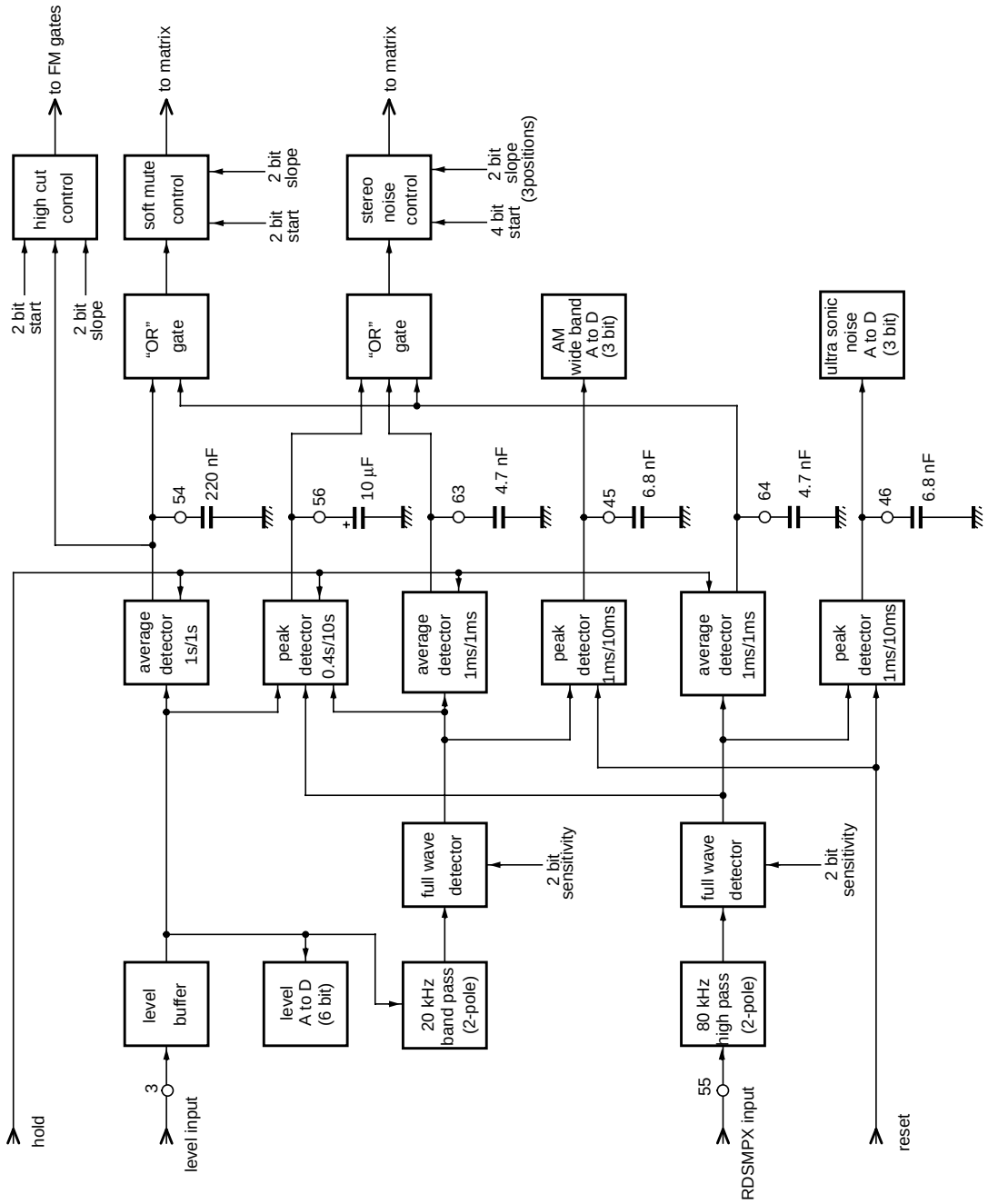


Fig.4 Block diagram of the weak signal processing

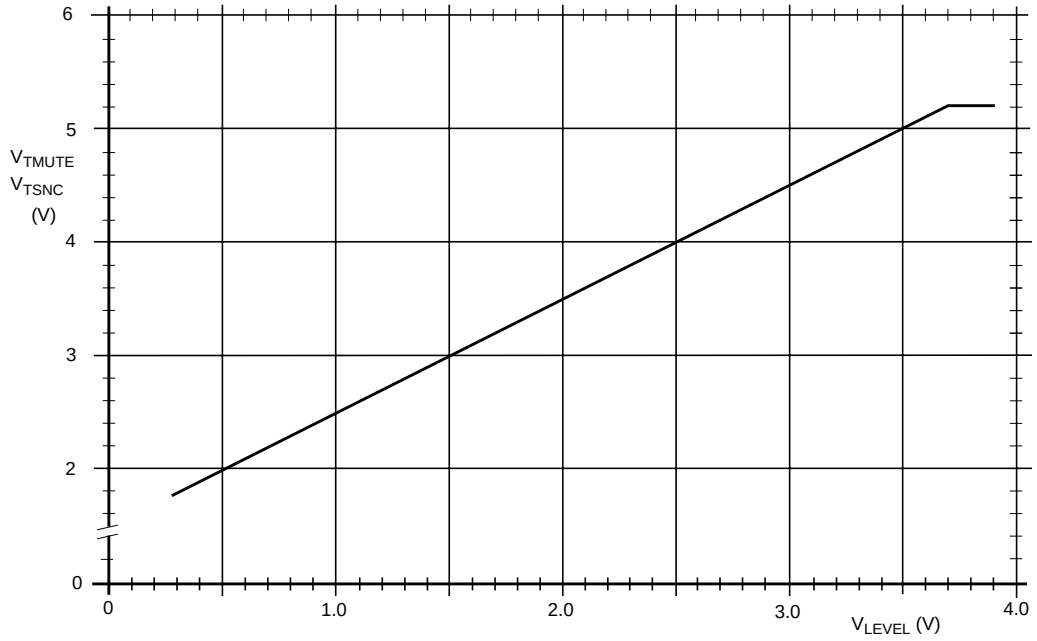
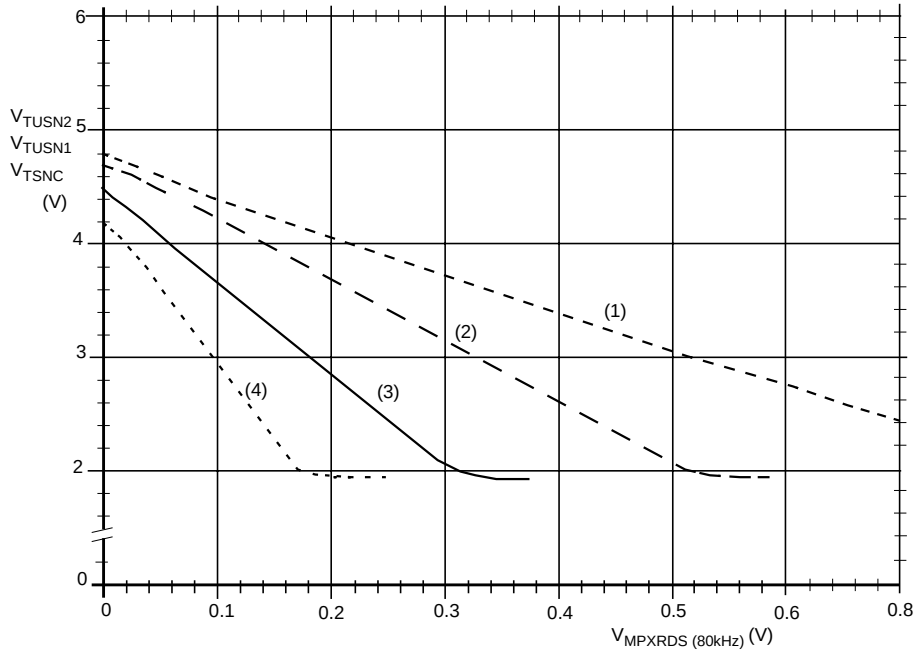


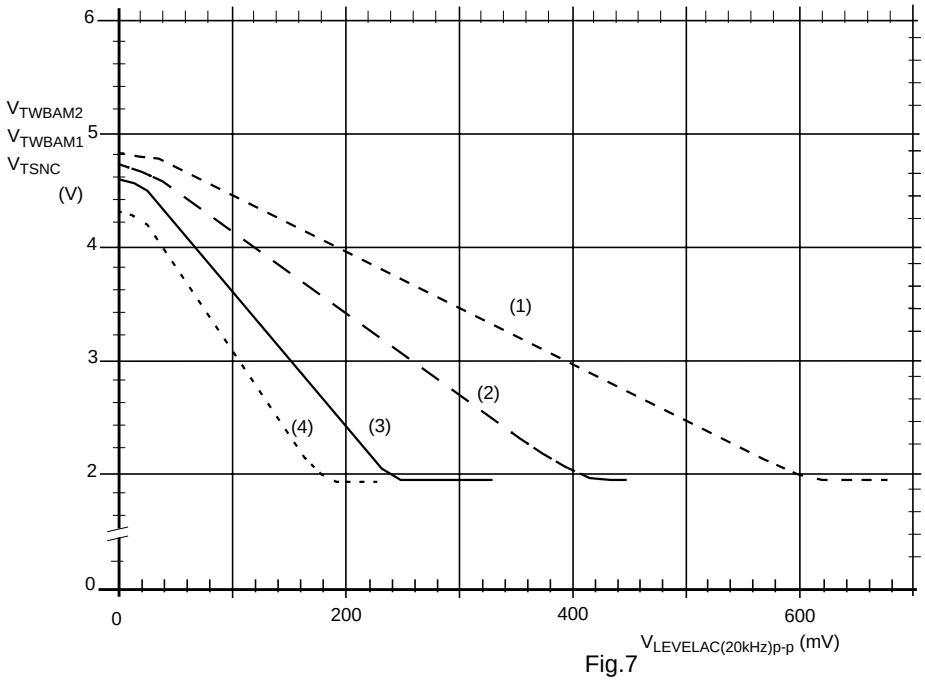
Fig.5 Muting average detector output voltage (pin54) versus level input signal (pin3)
Stereo noise control peak detector output voltage (pin56) versus level input signal (pin3)



data byte ALGN1

	USS1	USS0
(1)	1	1
(2)	1	0
(3)	0	1
(4)	0	0

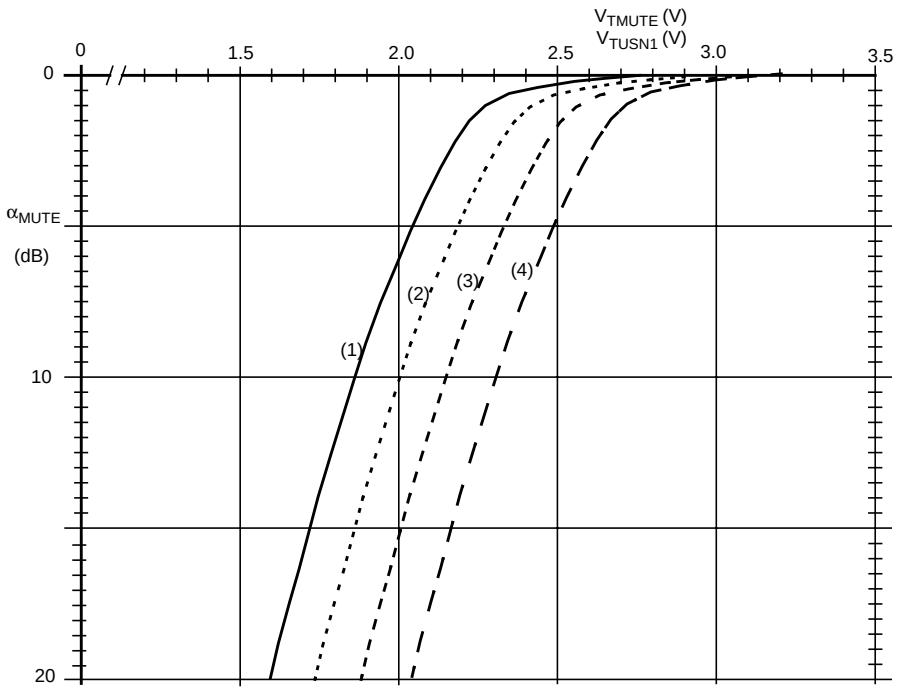
Fig.6
Ultra sonic noise average detector output voltage (pin64) versus MPX input voltage (pin55)
Ultra sonic noise peak detector output voltage (pin46) versus MPX input voltage (pin55)
Stereo noise control peak detector output voltage (pin56) versus MPX input voltage (pin55)



data byte ALGN1

	AWS1	AWS0
(1)	1	1
(2)	1	0
(3)	0	1
(4)	0	0

Fig.7
AM wide band average detector output voltage (pin63) versus level AC input signal (pin3)
AM wide band peak detector output voltage (pin45) versus level AC input signal (pin3)
Stereo noise control peak detector output voltage (pin56) versus level AC input signal (pin3)



data byte ALGN0

	MST1	MST0
(1)	0	0
(2)	0	1
(3)	1	0
(4)	1	1

Fig.8 Mute attenuation versus voltage at pins 54, 64 (TMUTE, TUSN1)
(fixed slope ==> data byte ALGN2: MSL1 = 1, MSL0 = 1)

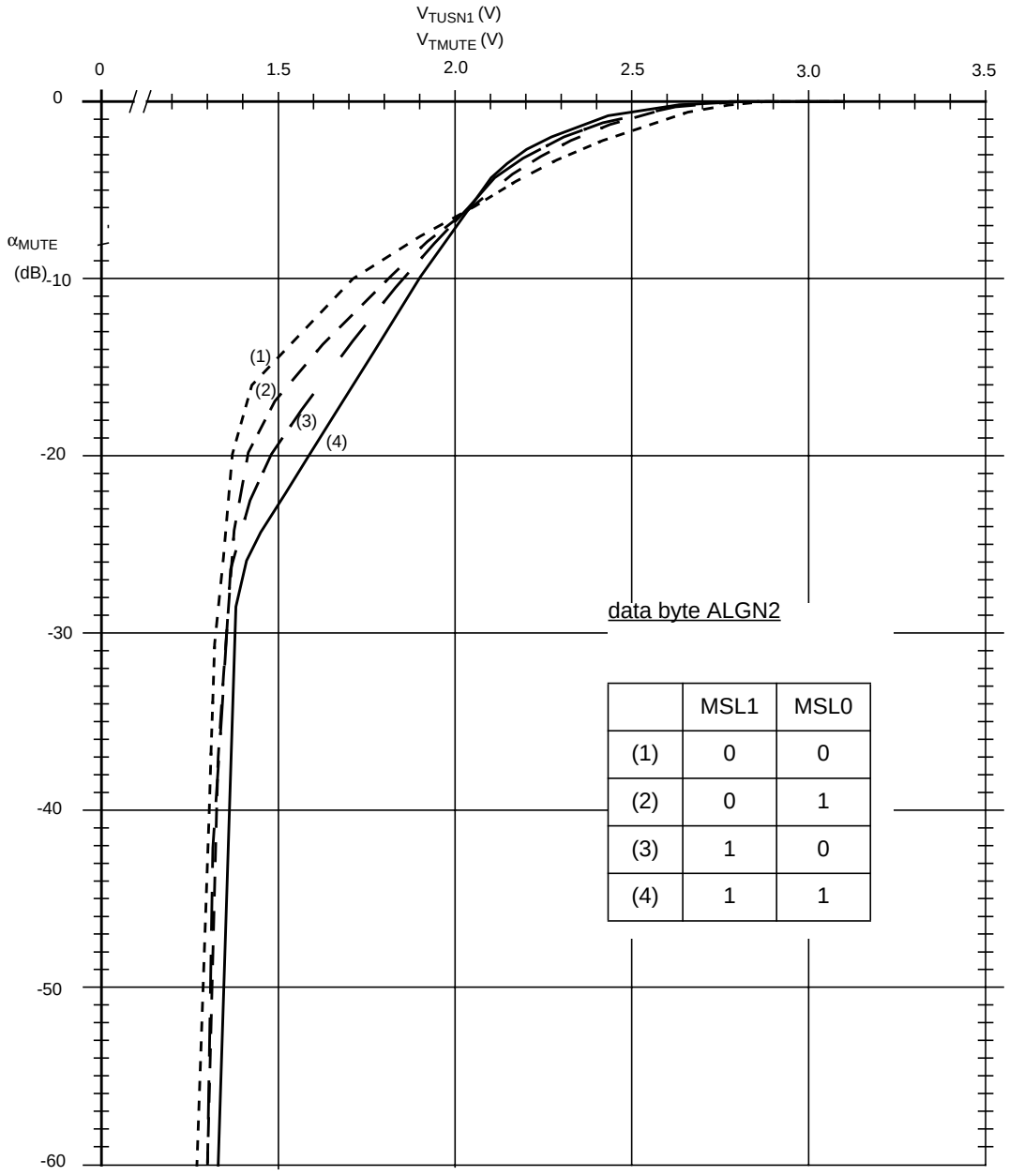
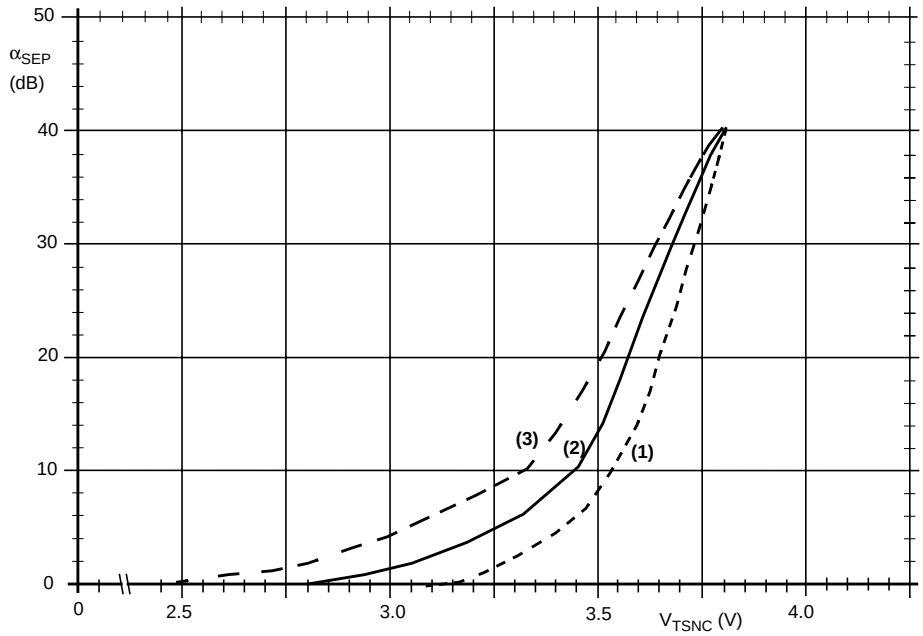


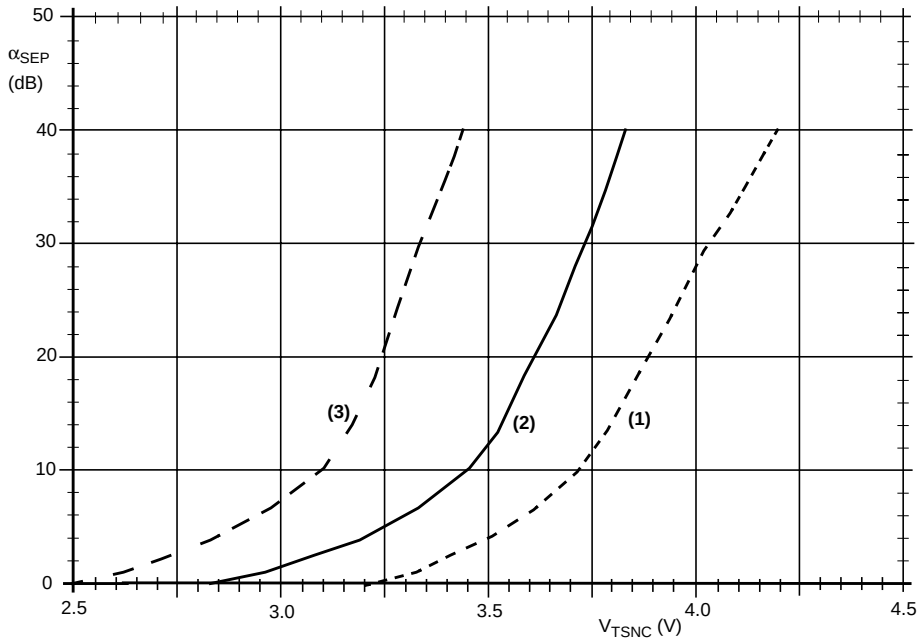
Fig.9 Muting attenuation versus voltage at pins 54, 64 (TMUTE, TUSN1)
(fixed start ==> data byte ALGN0: MST1 = 0, MST0 = 0)



data byte: ALNG2

(1) : SSL0 = 0, SSL1 = 0
(2) : SSL0 = 1, SSL1 = 0
(3) : SSL0 = 0, SSL1 = 1

Fig.10 Channel separation versus voltage at pins 56, 63, 64 (TSNC, TWBAM1, TUSN1)
(fixed start ==> data byte ALGN2: SST3 = 1, SST2...SST0 = 0)

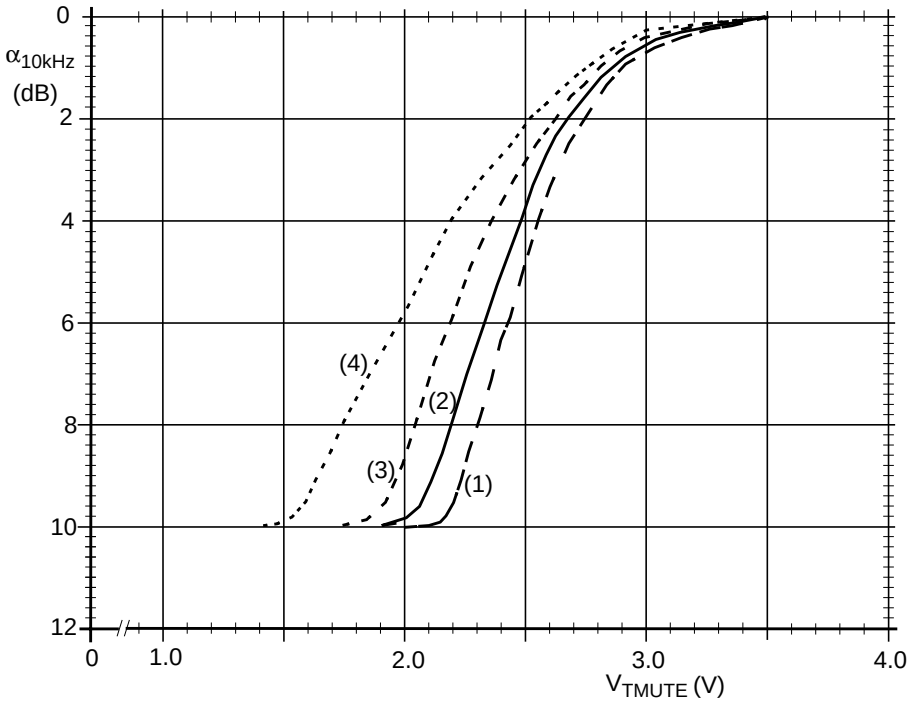


data byte ALIGN2

	SST3	SST2	SST1	SST0
(1)	1	1	1	1
(2)	1	0	0	0
(3)	0	0	0	0

SSL1 = 0, SSL0 = 1

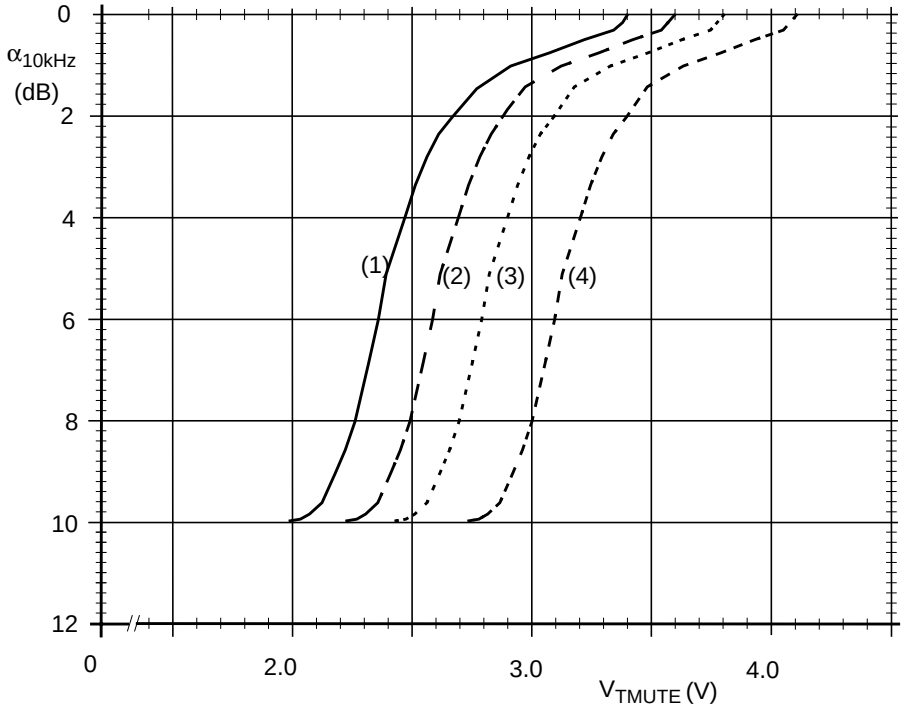
Fig.11 Channel separation versus voltage at pins 56, 63, 64 (TSNC, TAMWB1, TUSN1)
(fixed slope ==> data byte ALGN2: SSL0 = 1, SSL1 = 0)



data byte ALGN3
HST1 = 1
HST0 = 1

	HSL1	HSL0
(1)	1	1
(2)	1	0
(3)	0	1
(4)	0	0

Fig.12 10 kHz attenuation (high cut) versus voltage at pin54 (TMUTE)
(fixed start ==> data byte ALGN3: HST1 = 1, HST0 = 1)



data byte ALGN3
HSL1 = 1
HSL0 = 0

	HST1	HST0
(1)	1	1
(2)	1	0
(3)	0	1
(4)	0	0

Fig.13 10 kHz attenuation (high cut) versus voltage at pin54 (TMUTE)
(fixed slope ==> data byte ALGN3: HSL1 = 0, HSL0 = 0)

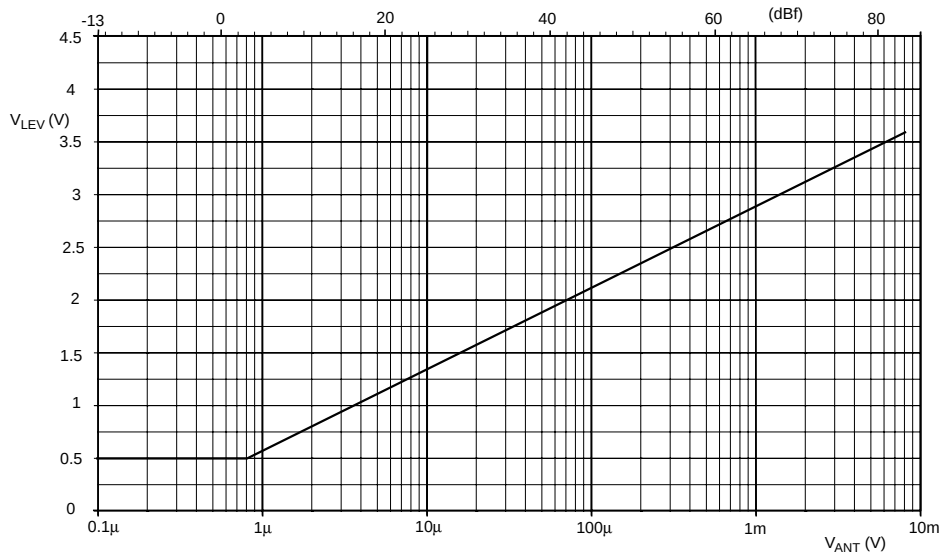


Fig.14 Expected level curve from receiver

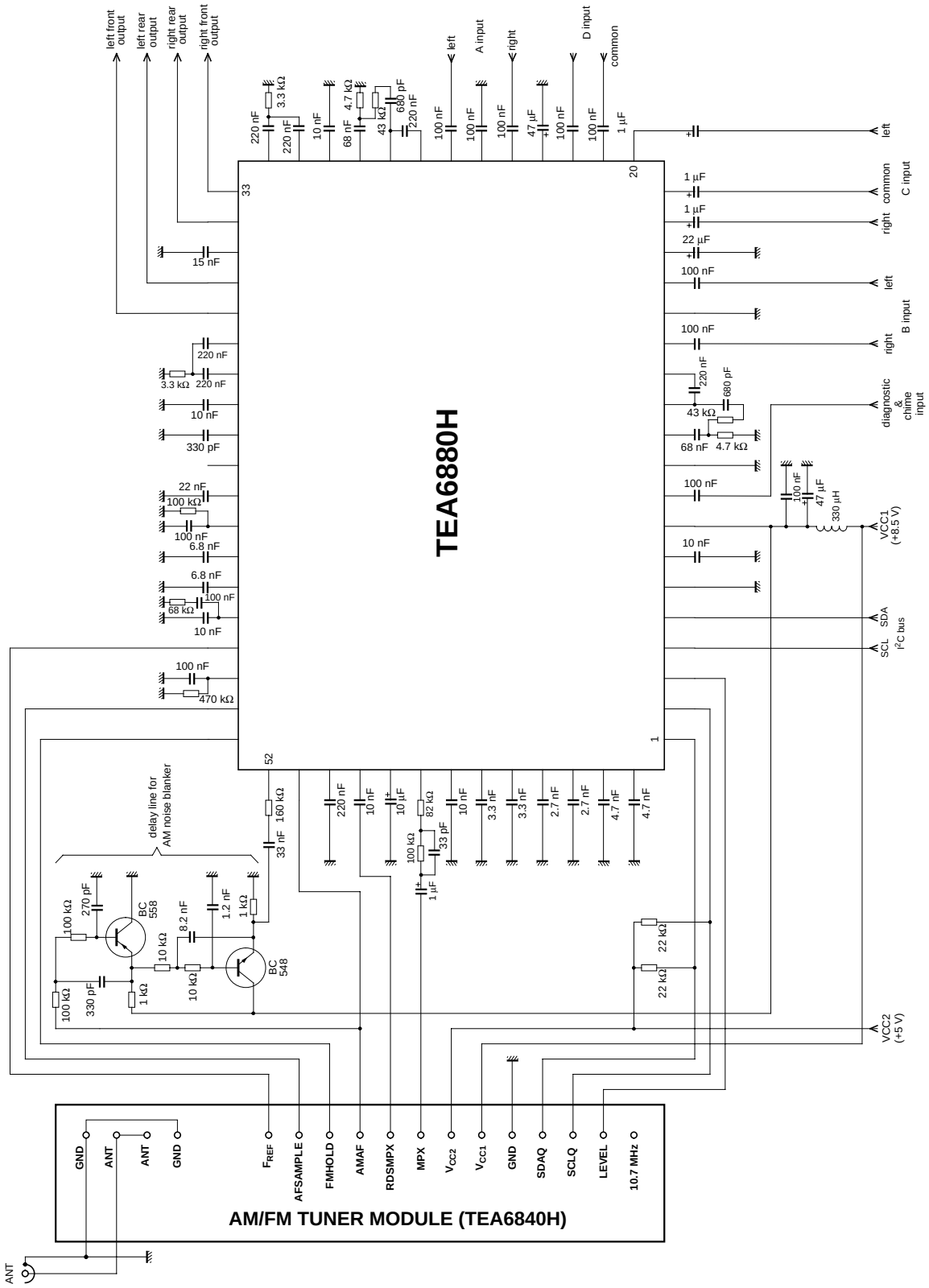


Fig.15 Application diagram of an AM / FM receiver with TEA6880H

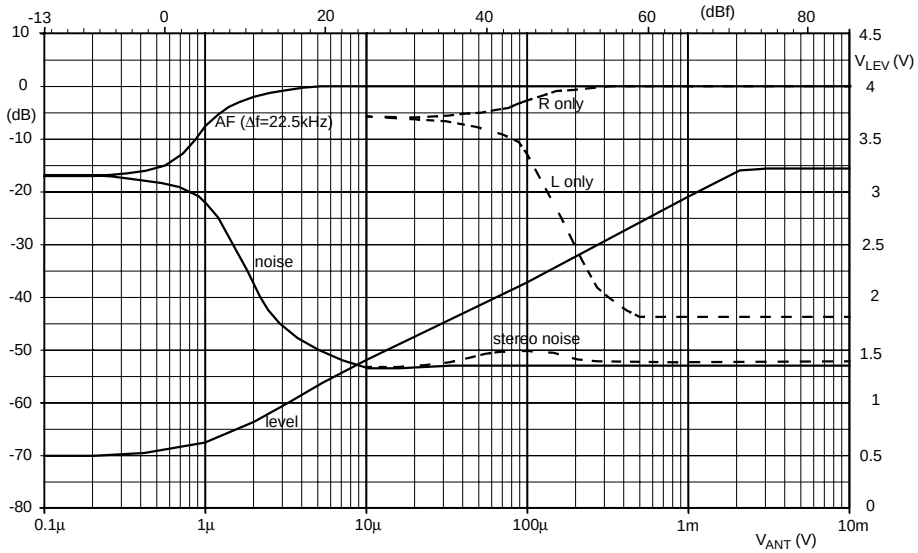


Fig.16 Weak signal behaviour versus antenna voltage

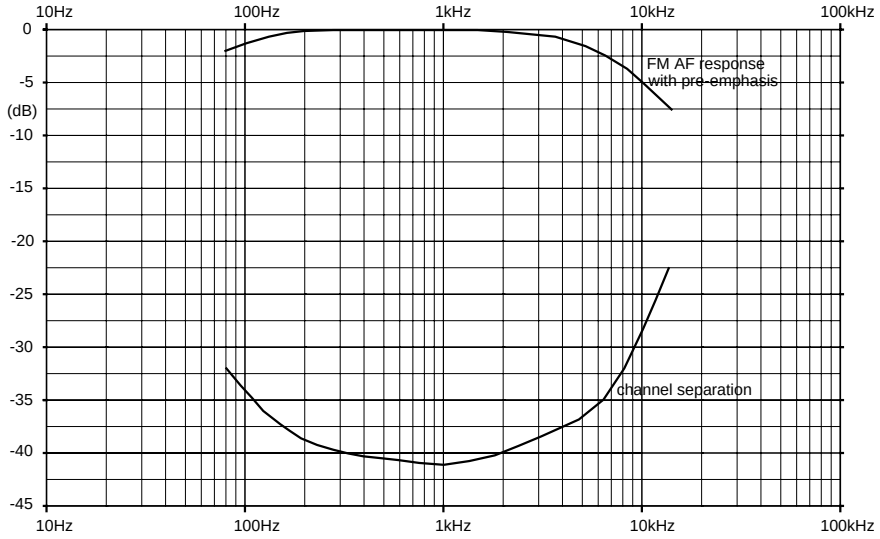


Fig.17 Audio response and channel separation (FM) versus audio frequency

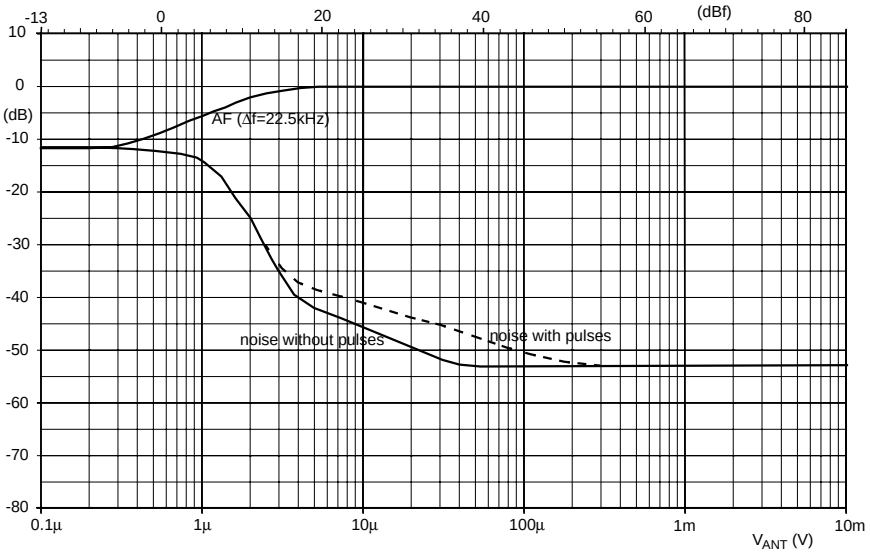


Fig.18 FM noise blanker performance versus antenna voltage

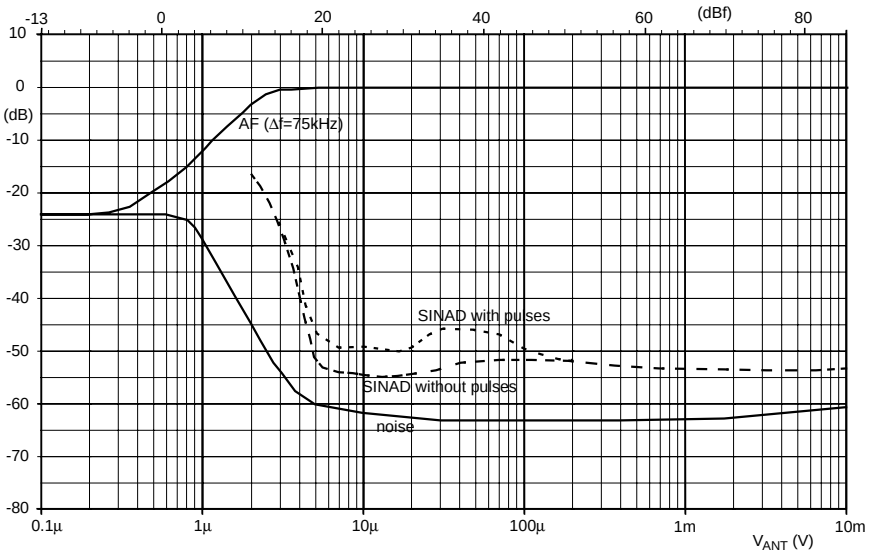


Fig.19 SINAD versus antenna voltage

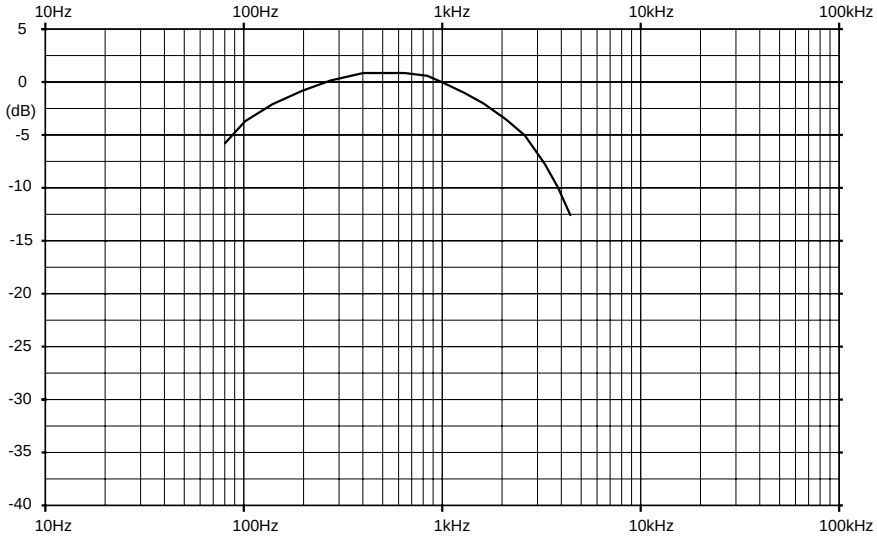


Fig.20 AM audio response versus audio frequency